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THE NEW PATENT REGIME: IMPLICATIONS FOR PATIENTS IN INDIA

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ABSTRACT

Recent patent-law changes in India's pharmaceutical industry provide opportunities to study changes of institutional and regulatory environments on innovation and social welfare in low-income markets. Researchers have debated the effects of India's new product-patent laws' effects on these trends. The authors cover the domestic characteristics and global competitiveness of India's pharmaceutical industry. They argue that Indian pharmaceutical companies have changed their decision-making in response to changed patent laws by moving from process to product research. However, the preliminary results indicate that these changes may have hurt domestic innovation. They conclude with strategic implications for the Indian pharmaceutical industry and highlight the need for research and public policy to establish optimal social returns from product-patent regimes. he analysis is based on secondary data published elsewhere. It also reviews the existing patent and drug control laws in India and how they have affected the growth and structure of pharmaceutical industry in the country.

Keywords:- patent, law, pharmaceutical, industry.

Pharmaceutical companies spend billions of dollars on research. It is estimated that, of every thousand potential drugs screened, only 4-5 reach clinical trials and only one is actually approved for marketing. Pharmaceutical companies patent the drugs that they develop and thereby obtain exclusive marketing rights; the costs of research and the profits due to the shareholders are recovered through appropriate pricing mechanisms from the patients who receive the patented drugs.

Internationally, drug patents and the exclusive marketing rights associated therewith are awarded for a period of 20 years; during this time, no other drug company is allowed to manufacture or market the same drug. After the patent expires, other companies are permitted to manufacture and market the drug; their brands are known as generic versions.

In the early 1970s, the Indian Patents Act was passed under the Indira Gandhi government to permit greater access of medicines at lower rates to the poor in the country. According to the Act, process patents but not product patents would be recognized. Expressed otherwise, India would award patents not to individual drugs but to the process whereby the drug was manufactured. This allowed Indian drug companies to manufacture the same drug using other processes (this is otherwise known as reverse engineering). As the Indian companies incurred little expenditure on research and development of new drugs, it became possible to make new drugs available to the country at affordable rates.

As India sought to improve its presence in the global market, it became clear that it could no longer protect domestic consumers in its patent policy. India is a member of the World Trade Organization. India therefore requires a new patent law to fulfil its obligations under the trade-related aspects of intellectual property rights (TRIPS). India became a member of the Paris convention and signed the Patent cooperation treaty with effect from December 7, 1998. Since then, amendments to the Patent Act were enacted in April 1999 and May 2002. The third amendment became due. The necessary bill to make the Indian Patents Act TRIPS-compliant was supposed to have been tabled during the 2004 winter session of Parliament; instead, an ordinance was passed on December 26, 2004, which came into effect on January 1, 2005. This ordinance modified the Indian Patents Act. This ordinance was itself modified and the Patents (Amendment) Bill was passed by the Lok Sabha and Rajya Sabha on March 22 and March 23, 2005, respectively. The President signed the bill on April 5, 2005, making it an Act of Parliament.

AT PRESENT, THE SCENARIO IN INDIA IS AS FOLLOWS

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India will respect product patents. However, the patents so respected will only be those issued in India.

Product patents will be respected for a period of 20 years from the time of application and not from the time of grant of the patent. About ten thousand applications for patents were pending with the government in 2005; these date back to 1995 and are designated as mailbox applications. It will take several years to screen all the applications and award patents as appropriate. This will increase the breathing space for Indian pharmaceutical companies and Indian consumers.

New applications for patents will also be processed; again, the grant of patent will be for 20 years from the date of application. This is in accordance with the Patent Cooperation Treaty which India has signed, which will make it possible for a new invention to be simultaneously patented in a large number of countries.

Other agencies interested in the product will be provided an opportunity to oppose the grant of patent. Both pre-grant and post-grant opposition will be entertained. In the December 2004 ordinance, pre-grant opposition had been emasculated to a written application with no further representation allowed on the part of the opposer; in contrast, under the previous patent act, pre-grant opposition was a more powerful procedure with the opposer having a right of audience to the proceedings involved in the grant of patent. With the new Patents Act of 2005, pre-grant opposition has been strengthened: more time has been allowed and the opposer has been given the right to be a party to the proceedings.

Even though the patent will be awarded with retrospective effect from the date of application, the implementation of the patent will only be with prospective effect. Thereby, generic versions of a drug will need to be withdrawn only after a patent is awarded and the companies manufacturing and marketing the generic drugs will not be retrospectively liable for having manufactured and marketed the drug. Furthermore, companies manufacturing products patented between 1995 and 2005 will be allowed to continue to do so after paying a reasonable royalty to the patent holder.

Companies sometimes resort to evergreening to extend the duration of their hold of a patent. Evergreening refers to the making of minor modifications in a drug structure or formulation. The December 2004 ordinance passed by the Indian government did not address evergreening. However, in the Patents Act of 2005, the definition of patentability was modified to prevent evergreening. As an example, this could mean that once-weekly fluoxetine and escitalopram would likely not be granted fresh patents to extend the marketing rights of the patent holders of fluoxetine and citalopram, respectively.

Fresh patents will not be granted for new indications for drug use; this was not explicitly prohibited in the December 2004 ordinance, but has been clarified in the Patents Act of 2005.

PROBLEMS THAT INDIAN PATIENTS MAY FACE

When the mailbox applications are cleared and patents awarded, newly-introduced generics in the Indian market may have to be withdrawn. This, for example, is why Indian brands of tadalafil have disappeared from the shelves. And, newer antipsychotic, antidepressant, antiepileptic and other drugs will be permitted to be marketed only by the patent holder. Costs to the patient will then inevitably rise. This scenario is feared but is by no means certain to occur as the international patents for almost all currently available drugs had been awarded before January 1, 1995, the cut-off date.

New drugs that emerge in the international arena will be available to Indian patients only from the patent holder. Again, the cost is almost certain to be high.

A SMALL CONSOLATION

A small consolation is that the bulk of the neuropsychiatric pharmacopoeia is out of patent and will remain available in the generic form.

DEFENCES AGAINST EXORBITANT PRICING AND UNAVAILABILITY

Tie-ups: Multinational drug companies have a weak presence in India: their drug basket is small, their marketing structure is weak and their domestic operations are limited. Multinational companies may need to tie-up with Indian companies for effective marketing. This may result in greater affordability to Indian patients. There is already evidence that Indian and multinational companies are exploring opportunities for mutual benefits. It is, however, unlikely that new drug prices will be as low as currently enjoyed by the Indian public.

Compulsory licensing: The Indian government has reserved the right for compulsory licensing; that is, providing Indian companies the privilege to manufacture and market a drug even before the expiry of the patent held for that drug. Compulsory licensing will be resorted to if the patent holder does not make the drug available to Indian patients or if the cost to Indian patients is too high. Compulsory licensing for export will also be resorted to, on similar grounds, to supply drugs to poor countries to meet their acute public health problems as per the TRIPS agreement of the Doha Declaration on Public Health.

By way of example: the Brazilian Government recently announced that it would break the patent on several retroviral drugs to prevent the financial collapse of its successful public health program which provided free medication to HIV/AIDS patients.

Article 31 of the TRIPS agreement provides for compulsory licensing without the authorization of the patent holder in the case of a national emergency or other circumstances of extreme importance or in cases of public, noncommercial use. This idea is also embodied in Section 92 of the Indian Patents Act of 1970. It is, however, uncertain that circumstances will arise which will make the Indian Government resort to compulsory licensing for psychotropic medication.

If compulsory licensing is to succeed, some absurdities in the existent Patent Act require to be removed. One absurdity is that a compulsory license cannot be awarded during the first three years of the grant of a patent. Another absurdity is that the applicant for a compulsory license is required to state the nature of his interest in the matter and the existing patent holder is allowed to oppose the grant of the application. While this is correct on the grounds of natural justice, it defeats the needs of emergency licensing. A third absurdity is that compulsory licensing is possible only for drugs which are patented in the country and not for those which are patented elsewhere. Pharmaceutical companies can therefore avoid compulsory licensing if they do not apply for a patent in India.

According to the provisions of the Patents Act of 2005, generic versions of patented drugs will be permitted to be manufactured and exported under a compulsory license to meet the major health needs of underdeveloped countries if the concerned countries issue a notification that the drug is required for the purpose.

Price control: The Indian Government has a list of drugs under price control. The exercise of this option may protect patients against exorbitant pricing. However, this option is unlikely to be exercised for newer psychotropic drugs unless the drugs have dramatic health benefits.

INDIRECT BENEFITS OF THE NEW PATENT REGIME

It will force the Indian pharmaceutical sector into greater efforts in research and development. Many of the pharmaceutical majors in India have already made large outlays in this area and have even applied for patents, though not necessarily for psychotropic drugs or even chemicals with therapeutic potential.

Outsourcing of laboratory research and clinical trials to India will increase, thereby facilitating the domestic processes for the approval of the marketing of a new drug. Even more importantly, outsourcing to India will lower research costs, thereby reducing the costs which will have to be recovered through pricing mechanisms. Finally, even bulk drug manufacture may be outsourced to India, which would further reduce the costs of the marketed product.

Small companies, many of which manufacture and market generic drugs of doubtful quality, will fold up.

Competition will eventually change from brand vs brand to drug vs drug.

UPDATE ON EVERGRENING

At present, there is a strong lobby trying to persuade the government to allow evergreening; that is, the patenting of molecules which differ slightly from the parent molecule. The argument is that molecules are patented very early during the process of drug discovery, but unique clinical characteristics or benefits are not discovered until much later, when clinical trials are conducted, if at all. Therefore, it is unreasonable to ask that unique characteristics of a slightly altered molecule be described at the time of the application for the patent, itself. Evergreening is not necessarily a disadvantage to India. For example, if evergreening is permitted, Indian companies may be able to develop and patent incremental advances on patented drugs.

A government-appointment committee on patent laws, headed by R. A. Mashelkar, a former chief of the Council for Scientific and Industrial Research, favored the grant of patents to all incremental innovations made to a drug, but not to frivolous evergreening. The report was widely interpreted to permit most forms of evergreening. The report also favored the grant of patents on microorganisms to make the Indian Patents Act TRIPS-compliant. The report was withdrawn in mid-February, 2007, after it was discovered that a part

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of the report was lifted, without acknowledgement and verbatim, from a paper published by a UK-based organization which had been funded by the pharmaceutical industry. In March, 2007, the Government requested the Mashelkar committee to revise and resubmit its discredited report.

On a related note, the patents act does not define how unique the new molecule must be; therefore, an element of subjectivity enters the decision-making process for the grant of a patent. In this context, the pharmaceutical industry is concerned that the officials involved in the grant of patents may not be sufficiently qualified to understand the nuances in molecular behavior that justify novelty and hence the grant of a patent.

UPDATE ON POSSIBLE PRICE CONTROL FOR PATENTED DRUGS

On January 26, 2007, the Union Ministry of Chemicals and Fertilisers announced that it was considering the formation of a committee which would suggest a system of price negotiation for patented drugs so that such drugs could be made available at an affordable price within the ambit of the National Pharma Policy. Without negotiated pricing, these drugs would not be given marketing rights in India. The committee would be headed by a Director (Chemicals) and would have representatives from all concerned ministries, including the ministries of health and commerce. The recommendations of the committee, if approved, would need to be made a legal requirement through an amendment of the Drugs and Cosmetics Act. A 7-member committee has now been set up.

NOTE ON GENE AND MICROORGANISM PATENTS

The USA allows gene patents; therefore, individuals or private organizations can own the intellectual rights on genes that determine health and disease. This will allow such individuals or organizations to permit or deny others the permission to research or even test for these genes or diseases. This adversely impacts upon medical progress and even individual healthcare. At present, over 20 human pathogens are privately owned, including Hemophilus influenzae and the Hepatitis C virus. The scandalous implications were well-discussed by Crichton.

CONCLUSION

Several ministries and departments are involved in the areas discussed in this report. The most important is The Controller of Patents, Government of India. This is the authority which will screen applications for patents, award patents and award compulsory licenses.

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ASIC Design of Radix-2,8-Point FFT Processor

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In split radix architecture, large sizes Fast Fourier Transforms (FFT) are decomposed into small independent computations to reduce storage burden. Radix-2, 8-point is one the popular choice in split radix for small independent computation. Authors proposes the FFT processor architecture for this small independent computation i.e. radix-2, 8-point FFT. This paper brief architecture comprising Butterfly Unit (BU), register set and controller. The novelty of this architecture is that it replaces the series of Processing Elements (PE) by single BU. BU computes two halves of the computations concurrently. Arithmetic computations are performed in floating point form to overcome the nonlinearities. All computations are controlled by tailored instruction set. All instructions are of same size and have same execution time. Twiddle constants are implicitly available in the instruction. Internal computations are stored in register set to avoid the load and store operations with memory. The mean square error of the computation is reduced by 41.95% and 55.76% in magnitude and phase respectively as compared with computations performed by rounding the twiddle constant. This FFT processor is synthesized, placed and routed for 45 nm technology of nangate open cell library. The BU of this architecture is 18.89% smaller and 5.13% faster as compared with smallest and fastest BU reported previously. The hardware cost metric i.e. AT^2_{norm} D_p mm^2 ns^2 mW of proposed processor is 1.37. This cost metric is also 32.51% less as compared with the previous work.

Keywords: Butterfly Unit, Fast Fourier Transform, Fused Floating Point Addition–Subtraction, Non-redundant arithmetic

Introduction

Digital Signal Processor (DSP) widely use FFT for signal processing in variety of fields such as entertainment devices, wireless broadband communication system, microwave access (Wi Max), long term evolution, image processing and biomedical signal processing. In the past decade, various pipelined FFT processor architectures were presented on split radix in which large size FFTs were decomposed into small independent computations. Radix-2, 8-point FFT computation was majorly used as the one of decomposition in split-radix architectures. The decomposition of large size FFT helped to balance the functionality and increases the performance of FFT processor. The performance of the processor is also increased by eliminating memory to store the intermediate computations. The pipeline architectures were of mixed radix multipath delay feedback,[1,2] ring structured multiprocessor,[3] scalable array structure,[4] single delay feedback,[5] fixed point reconfigurable architecture[6] and parameterisable architecture for memory based FFT algorithm.[7] On the other hand, pipeline architectures consist of an interleaved series of computational elements and data storage elements i.e. processing elements (PE). Computational elements known as butterfly unit (BU) are responsible for performing multiplication and addition. Hence the architecture of BU is also an important unit to decide the performance of FFT processor. In this decade, various BUs were proposed based on floating point arithmetic to overcome nonlinearities such as overflow of number range, rounding errors, aliasing errors and coefficient errors. However, floating point arithmetic has sluggish nature. To improve speed and to reduce area of consumption, various arithmetic hardware were proposed by sharing common logic,[8] dual path pipeline,[9] multi-operand adder[10] and redundant arithmetic.[11,12] Lookup table enabled multiplier, hash indexing function[13] and Gauss-Eisenstein representation[14] was also used for arithmetic operations. This paper proposes architecture of radix-2, 8-point FFT processor for small independent

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computation suitable in split radix architectures. The novelty of this architecture is that single BU free from series of processing elements (PE), computes two halves of the computation concurrently. This BU also computes FFT in time domain as well as in frequency domain. Dual path fused floating point addition-subtraction (DFFAS) and two floating point multipliers (FMULT) are the major entities of BU.

The computation program based on radix-2 algorithm is written by author and stored in program memory. This paper briefs on the following:

1 Architecture of FFT processor.
2 BU, comprising DFFAS.
3 Tailored instruction set to perform arithmetic operations.
4 Comparison of FFT computational error occurred using floating point against the fixed-point representation of twiddle constant.

Architecture of Proposed FFT Processor

Architecture of proposed FFT processor is shown in Fig.1. BU, three register files, multiplexers and controller are the main entities in proposed FFT processor. Features of this FFT processor are

- It is16-bit processor.
- BU performing addition and multiplication on floating point numbers represented in 16 bits simple 2's complement form.
- Tailored instruction set. All instructions have equal length i.e., 20-bit and same execution time.
- It has three register files named as main, real and imaginary. Each register file consists of 8, 16-bit registers.

BU comprises of DFFAS, multiplexers and FMULT. This BU is responsible to perform arithmetic operations. Register files are used to hold the input sequence, intermediate computational operand and output sequence. 4:1 multiplexer is used to select the operands for arithmetic operations. 2:1 multiplexer enables data transfer between two registers.

The program memory is interfaced with the FFT processor using interfacing signals. These interfacing signals are shown in Table 1. The interfacing signals consist of 20-bit data bus, 6-bit address bus, clock input and reset input. Controller writes the address of program memory to fetch the instruction. The fetched instruction is decoded by controller. After decoding instruction, controller generates controls signals as shown in Table 2. The control signals WREN, WAD and RAD are used by register files to perform write and read operation. Register file has one input data bus and two output data buses. The input data bus is used to perform write operation. The register write operation is enabled by asserting WREN signal. The write operation is performed on the register whose address is available in WAD. Simultaneously, two

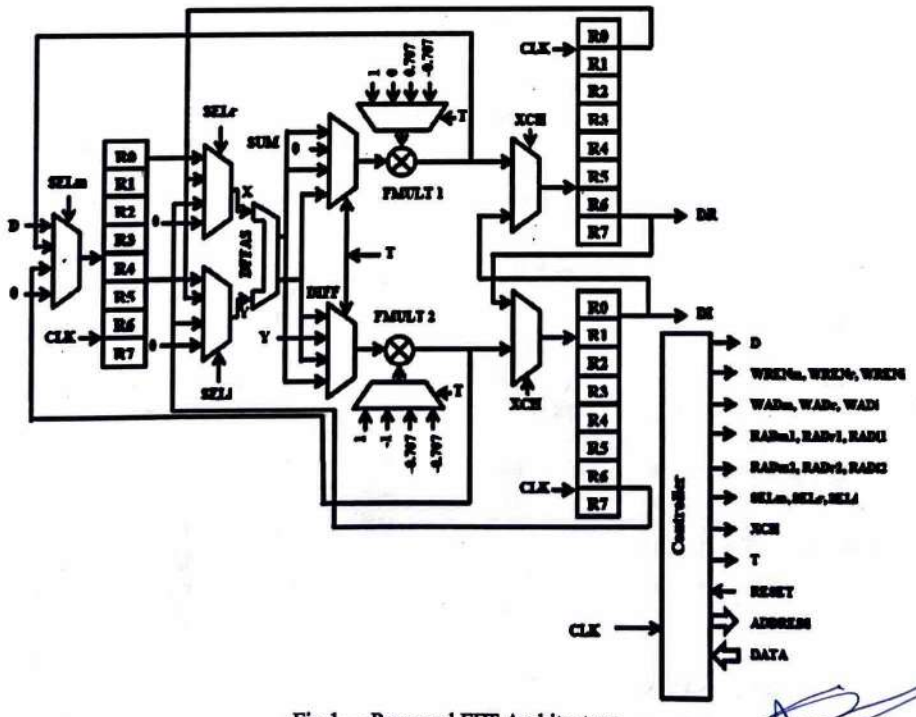

Fig.1 — Proposed FFT Architecture

registers are read through output data buses. Register file has two additional input buses i.e., RAD 1 and RAD 2 to perform read operation. RAD 1 and RAD 2 holds the addresses of two registers to perform read operation on them.

The signal XCH is used to copy the information from register available in real register file to register available in imaginary file and vice-versa. The register addresses are shown in Table 3. The Rm denotes the register from main file, Rr denotes the register from real file and Ri denotes the register from imaginary file.

The main register file stores the immediate data sequence (D), products from multipliers and 0d. They are selected through the select line SELm. Similarly, the operands X and Y for DFFAS are selected through SELr and SELi respectively. This operand selection is listed in Table 4.

The twiddle constants and butterfly operations are selected by T. The twiddle constants selected through T are listed in Table 5.

Table 1 — Details of Interfacing Signals

Symbol	Status	Description
DATA	Input	20-bit data bus.
ADDRESS	Input	6-bit address lines.
Clock	Input	Clock signal for synchronization of the operation.
Reset	Input	Active high synchronous reset. On reset, initializes the operation at default level. Address lines are initialized at 000000b and others signals are maintained the state at high impedance level.

Table 2 — Signals Generated by Controller

Symbol	Width	Description
D	16	A data line carries the immediate data bits.
WREN	1	Register write enable: Active high signal enables the register to write the information in specified register.
WAD	3	Register write address: Denotes the address of register to write the information in it.
RAD	3	Register read address: Denotes the address of register to read information from it.
SEL	2	Select lines to select the operand.
XCH	1	Enables the data transfer between two register files. XCH= 0b transfer the data from Rr to Ri XCH= 1b transfer the data from Ri to real Rr
T	2	Select the stage of FFT operation.

Table 3 — Registers Address for Read, Write Operations

WAD	RAD	Rm	Rr	Ri
000b	000b	R0	Rr0	Ri0
001b	001b	R1	Rr1	Ri1
010b	010b	R2	Rr2	Ri2
011b	011b	R3	Rr3	Ri3
100b	100b	R4	Rr4	Ri4
101b	101b	R5	Rr5	Ri5
110b	110b	R6	Rr6	Ri6
111b	111b	R7	Rr7	Ri7

Instruction Set

Instructions are available to perform the trivial as well as complex arithmetic on operand. Instruction set is shown in Table 6. The 16-bit immediate data is indicated by "nn". SRC indicates the source and DST points the destination. X denotes the BU stage. Twiddle constants are implicitly available in the instruction. Here the memory is not used for load and store operation. The source and destination address of the registers are mention in the instruction itself. This saves the load and store time with off chip memory. Each instruction takes 2 cycles to decode and execute. Here data is represented in 16-bit simple 2's complement form.[15] All floating-point operations are performed as described by Kulkarni *et al.*[16]

Butterfly Unit

BU design reported by Kulkarni *et al.*[16] uses fused floating-point addition-subtraction (FFAS), FMULT and four 4:1 multiplexer. However, in this FFAS unit, exponent comparator, compares two exponents by taking difference between them. If this difference is too large, then the mantissa of the number having smaller exponent will be insignificant and truncated after the mantissa shifted more than 16 bits. Hence this logic sets operand having smaller exponent to zero value. Therefore, additional path is proposed in the FFAS design to skip FFAS algorithm and result is

Table 4 — Operands for Register Write in Main Register File and Operands for DFFAS

Operand for main Register file		Operands for DFFAS			
SELm	Operand	SELr	X	SELi	Y
00	Immediate data sequence (D)	00	Rm	00	Rm
01	Output from FMULT 1	01	Rr	01	Rr
10	Output from FMULT 2	10	Ri	10	Ri
11	0000 H	11	0000H	11	0000H

Table 5 — Twiddle Constants

W_N^{nk}	Twiddle Constant
W_8^0	1
W_8^2	-j
W_8^1	$0.707 - j0.707$
W_8^3	$-0.707 - j0.707$

Table 6 — Instruction Set

Instruction	Description
Load Rm, ##nn	Load immediate 16-bit data in main register
BU X SRC1, SRC2, DST1, DST2	BU stands for butterfly computation. X indicates the stage (0 to 3), SRC and DST from Rm, Rr or Ri. BU0 R0, R1, Rr0, Ri0 perform R0±R1, store the sum in Rr0 and difference in Ri0. However, SRC1/DST1 is either Rm or Rr. Similarly, SRC2/DST2 is either Rm or Ri.
BU X #0, SRC2, DST1, DST2	There is a special case in which the SRC1 is '0' and DST1 and DST2 are same as described above.
BU X SRC1,#0,DST1,DST2	There is also a special case in which the SRC2 is '0' and DST1 and DST2 are same as described above
Mov Rr,Ri	Copy the contents of Ri in to Rr.
Mov Ri,Rr	Copy the contents of Rr, Ri.
Out Rr,Ri	Read the contents of Rr, Ri
Halt	Termination of Program

Table 7 — Decision Table for Special Cases

Input X,Y	Sum	Difference
X ≠ 0 ,Y≠ 0	X+Y	X-Y
X ≠ 0 ,Y= 0	X	X
X =0 ,Y≠ 0	Y	-Y
X =0 ,Y= -1	Y	-Y = 1
X = 0 ,Y= 0	0	0

set to predefined value. Operands -1d or 0d or 1d are the frequently used coefficient in FFT computation. Hence additional path for operands -1d,0d and 1d is introduced. Additional path comprises magnitude comparator and multiplexers. Magnitude comparator compares the operand with -1d, 0d and 1d. The output of comparator enables the multiplexers to set sum/difference to predefined value as mentioned in decision Table 7. The FFAS design with this additional path is named as dual path fused floating point addition-subtraction (DFFAS) as shown in Fig. 2. Floating point addition-subtraction perfomed by DFFAS for the operands other than –1d,0d and 1d is similar to FFAS designed by Kulkarni *et al.*[16] This DFFAS is proposed at the place FFAS in BU designed by Kulkarni *et al.*[16] This new proposed BU is shown in Fig. 3.

The signal flow graph (SFG) of radix-2, 8-point FFT is shown in Fig. 4. It has regular and symmetric structure. This SFG has three stages. In stage 1, a single butterfly operation is present. In stage 2, two butterfly operations are present. Similarly, in stage 3, four butterfly operations are available. Therefore, a single BU is designed to perform all butterfly operations instead of using different processing elements for each stage butterfly operation. The twiddle constants required for butterfly operations are shown in Table 5 previously.

At the first stage, $W_8^0 = 1$. Hence trivial butterfly operation is performed on X and Y. They are added and subtracted. This butterfly operation is initiated by T = 00b. The sum and difference of X and Y are available at output R and I respectively. Second stage of SFG has two butterfly operations. Here $W_8^0 = 1$ and $W_8^2 = -j$. Hence trivial butterfly operation remained same. Another butterfly operation is performed with input Y. Input Y is multiplied by – 1. This second butterfly operation is selected when T= 01b. The product of multiplication is available at the output I. Third stage of SFG has four butterfly operations. The butterfly operations with twiddle constant $W_8^0 = 1$ and $W_8^2 = -j$ are similar to previous stages. The additional two butterfly operations are performed on input X and Y. In this stage input X denotes the real part and Y denotes the complex part of the intermediate computation available from previous stage. When T = 10b, intermediate computation from previous stage is multiplied by $W_8^1 = 0.707 - j0.707$. The similar complex multiplication of $W_8^3 = -0.707 - j0.707$ with intermediate computation is performed when T=11b. The real part of multiplication is available at output R and imaginary part of it is available at output I. The operational methodology[16] for butterfly operations is shown in Table 8.

FFT Computation and Error Analysis

FFTs of input sequences shown in Table 9 are computed using designed FFT processor. The computation is performed using decimation in time (DIT) as well as decimation in frequency (DIF). A computational program is written using the tailored instruction set shown in Table 6. The binary file of computational program is the part of design to test the functionality. Verilog entity of this binary file is named as program memory. Xilinx 14.7 is used to simulate the computational program. The FFTs of same input sequences are also computed by rounding the twiddle factors on proposed processor. To validate the result, FFTs of sequences are also

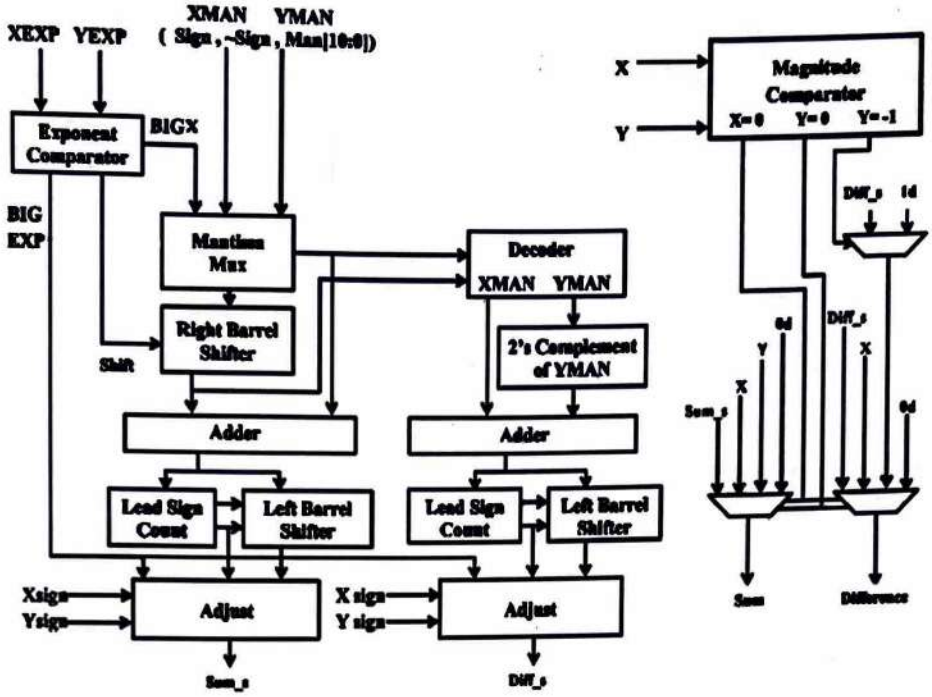

Fig. 2 — Dual Path Fused Floating Point Addition-Subtraction

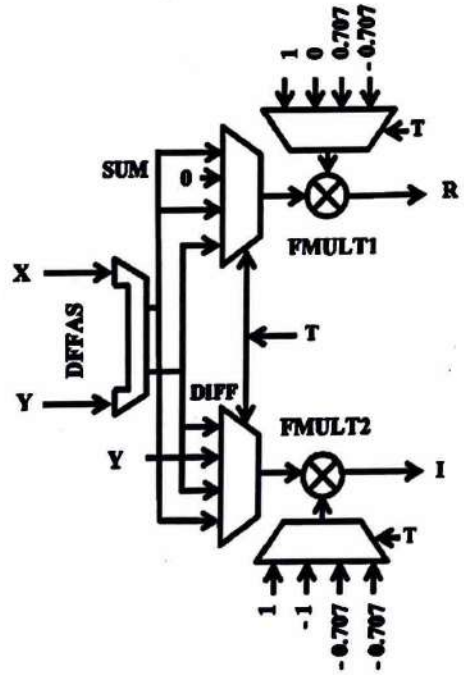

Fig. 3 — Radix-2,8-point Butterfly Unit

simulated using Scilab. The magnitude X[k] and phase < X[k] of FFT output is used to compare the result. The magnitudes and phases of the FFT ouputs are calculated using Eqs 1 & 2.

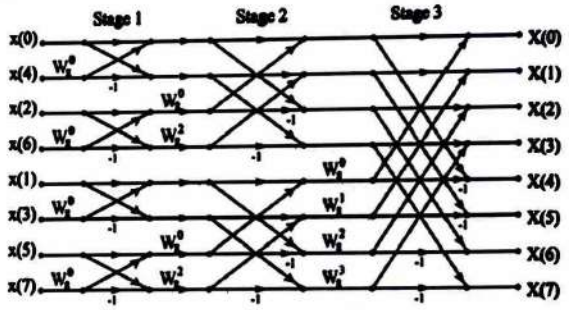

Fig. 4 — Signal Flow Graph for Radix-2,8-Point FFT

$$|X[k]| = \sqrt{X_{real}^2 + X_{imaginary}^2} \quad \ldots(1)$$

$$< X[k] = \tan^{-1} \frac{X_{imaginary}}{X_{real}} \quad \ldots(2)$$

These calculated magnitudes and phases values are compared with their Scilab simulated values. The comparison is in terms of mean square error (MSE). MSE is calculated using Eq. 3.

$$MSE = \frac{1}{N} \sum_{k=0}^{N-1} E(|X(k) - X_{calculated}\ (k)|)^2 \quad \ldots(3)$$

$X(k)$ is simulated value using Scilab. $X_{calculated}\ (k)$ is calculated value using proposed FFT processor. N represents the numbers of computations. The MSE is calculated for each sequence without and with rounding the twiddle constant as shown in Table 9. The MSE, without

Table 8 — Operational Methodology

Inputs	Stage	Twiddle factor	FMULT 1 Inputs	FMULT 2 Inputs	Output R	Output I
X,Y	I T=00	$W_8^0 = 1$	$X+Y,1$	$X-Y,1$	$X+Y$	$X-Y$
$0,Y$	II T=01	$W_8^2 = -j$	0,0	$Y,-1$	'0'	$-jY$
$X+jY$	III T=10	W_8^1 $= 0.707$ $-j0.707$	$X+Y$, 0.707	$X-Y$, -0.707	Real Part	Imaginary Part
$X+jY$	III T=11	W_8^3 $= -0.707$ $-j0.707$	$X-Y$, -0.707	$X+Y$, -0.707	Real Part	Imaginary Part

rounding and with rounding of twiddle constants are 3.16 and 5.45 respectively for magnitude. Similarly, the MSE are 0.29 and 0.66 without and with rounding the twiddle constants respectively for phase. The proposed architecture reduces the MSE by 41.95% and 55.76% in magnitude and phase respectively as compared against its simulation performed by rounding the twiddle constant. The standard deviation and standard error are also computed for MSE. The standard error for magnitude is 2.83 in case of twiddle constants are rounded off and 1.14 otherwise. Similarly, the standard errors for phase values are 0.16 and 0.39 without and with rounding the twiddle constant respectively. Hence the proposed architecture reduces the standard error by 59.71% and

Table 9 — MSEs of FFT Computations

Sr No.	Input Sequence	Domain	MSE in Magnitude		MSE in Phase	
			Without Rounding	With Rounding	Without Rounding	With Rounding
1	1,2,3,4,4,3,2,1	DIT	0.006563	0.018	0.044063	0.353
2	1,2,3,4,4,3,2,1	DIF	0.003525	0.018	0.054141	0.349741
3	1,1,1,1,-1,-1,-1,-1	DIT	0.032038	0.023	0.02905	0.966077
4	1,1,1,1,-1,-1,-1,-1	DIF	0.028061	0.05698	0.004449	0.348237
5	1,-1,1,-1,0,0,0,0	DIT	0.006875	0.0065	0.00897	0.039812
6	1,-1,1,-1,0,0,0,0	DIF	0.007069	0.006432	0.006554	0.039812
7	2,1,2,1,2,1,2,1	DIT	0	0	0	0
8	2,1,2,1,2,1,2,1	DIF	0	0	0	0
9	1,2,3,2,1,2,3,2	DIT	0	0	0	0
10	1,2,3,2,1,2,3,2	DIF	0	0	0	0
11	1,1,1,1,0,1,1,1	DIT	0	0	0	0
12	1,1,1,1,0,1,1,1	DIF	0	0	0	0
13	1,2,4,8,16,32,64,128	DIT	29.00963	59.14134	0.007001	0.034374
14	1,2,4,8,16,32,64,128	DIF	28.23196	62.15168	0.005252	0.035111
15	128,64,32,16,8,4,2,1	DIT	7.722965	15.83844	0.001468	0.129015
16	128,64,32,16,8,4,2,1	DIF	23.21319	15.83844	0.013673	0.02153
17	64,32,16,8,4,2,1,0	DIT	1.931382	3.998601	0.001428	0.020782
18	64,32,16,8,4,2,1,0	DIF	1.720276	3.998601	0.000643	0.020782
19	0,1,2,1,0,-1,-2,-1	DIT	0.040316	0.10663	0	0.61685
20	0,1,2,1,0,-1,-2,-1	DIF	0.047816	0.10663	0.308644	0.61685
21	2,1,0,-1,-2,-1,0,1	DIT	0.301449	0.462885	0	0
22	2,1,0,-1,-2,-1,0,1	DIF	0.328785	0.462885	0.063263	0
23	0,1,2,3,4,5,6,7	DIT	0.124693	0.103462	0.019086	0.040108
24	0,1,2,3,4,5,6,7	DIF	0.288528	0.103462	0.083398	0.040108
25	7,6,5,4,3,2,1,0	DIT	0.124693	0.103462	0.776286	0.040108
26	7,6,5,4,3,2,1,0	DIF	0.126876	0.103462	0.023278	0.040108
27	16,8,4,2,1,0.5,0.25,0	DIT	0.638105	0.13083	0.024978	0.047688
28	16,8,4,2,1,0.5,0.25,0	DIF	1.026858	0.672341	0.029083	0.105215
29	-1,-1,-1,-1,1,1,1,1	DIT	0.030933	0.288264	3.609475	10.85544
30	-1,-1,-1,-1,1,1,1,1	DIF	0.066433	0.025874	3.687191	5.137126
		Mean	3.168634	5.458873	0.293379	0.663262
		Standard Error	1.14	2.83	0.16	0.39
		Standard deviation	8.18	15.53	0.92	2.14

58.97% in magnitude and phase respectively as compared against the fixed point representation of twiddle constant.

Hardware Implementation and Comparison of Result

Verilog codes of DFFAS, BU and proposed architecture of FFT processor are synthesized and placed using Mentor-Graphics - Oasys for 45 nm technology of nangate open cell library. Operating conditions are set to typical values. Authors have also synthesized the Verilog codes of the discrete design of floating point addition-subtraction and FFAS. In discrete design, common logic i.e., exponent comparator, mantissa mux and right barrel shifter are not shared. Similarly, in FFAS, no additional path is used. The comparative statistics of synthesized result is shown in Table 10. Discrete addition-subtraction design consumes 11422 μm^2 area with the delay of 1.47 ns. Similarly, FFAS and DFFAS design contributes area 10330 μm^2 and 10836 μm^2 respectively. FFAS and DFFAS design causes delay of 1.56 ns and 1.63 ns respectively. Area and delay of DFFAS are increased by 4.66% and 4.06% respectively as compared with FFAS.[16] This addition in area and delay is due to the additional pathused in DFFAS. Proposed BU design reports a delay of 3.51 ns with placement area of 20423 μm^2. Comparison of butterfly designs with previously reported work[8,10,11,16] is shown in Table 11. The proposed BU design reduces area by 14.58% with the additional delay of 1.99% as compared with authors previous work.[16] Similarly, the proposed BU design reduces area by 18.89% and delay by 5.13% as compared with the previous work reported by Kaivani *et al.*[10]. In addition to this, work reported by Kaivani *et al.*[10] computes one halves with five operand adder and two dot products. However proposed BU computes two halves with single DFFAS and two FMULT. The trade-offs between area and delay are usual conflicts. Hence the second order area time complexity parameter AT^2 i.e. Area × $Time^2$ is mentioned in comparison. It is worth mentioning that proposed BU design has smallest AT^2. The work reported by Kaivani *et al.*[11] is based on redundant algorithm. Here additional logic is required to convert the data available in non-redundant form to redundant form and vice-versa. Redundant to non-redundant logic contributes the additional delay and area.

BU of proposed FFT processor takes two cycles are required to complete one butterfly operation which one more cycle to write back the result in register file. However, the BU designed by Noor *et al.*[13] takes 12 cycles to complete one butterfly operation and additional 6 cycles for memory read, write back and scaling process. Therefore total 18 cycles to complete one BU operation and is too large as compared with the proposed design. The Mentor Graphics Oasys-Nitro flow is used to place and route the proposed architecture of FFT processor. The logical hierarchical placement details of proposed FFT processor in Nitro is shown in Table 12. Design summary is shown in Table 13. Synthesized, placed and routed results show that proposed processor has die area of 37251 μm^2 at 60.86% chip utilization.

Table 10 — Comparative Statistics of Floating-point Addition and Subtraction

Parameter	DFFAS Proposed	Discrete Addition –subtraction[16]	FFAS[16]
Technology	Nangate Open Cell Library 45nm	Nangate Open Cell Library 45nm	Nangate Open Cell Library 45nm
Area (A) in (μm^2)	10836	11422	10330
Delay (T) in (ns)	1.63	1.47	1.56
AT^2 in (mm^2 ns^2)	0.028	0.024	0.025

Table 11 — Comparison of Butterfly Unit

Parameter	Proposed Design	SwartzlanderJr *et al.*[8]	Kaivani *et al.*[10]	Kaivani *et al.*[11]	Kulkarni *et al.*[16]
Technology	Free PDK Nangate Open cell 45nm Lib	45nm Bulk CMOS Standard Lib	45nm Opennangate	STM CMOS 90nm Liband Scaled to 45nm	Free PDK Nangate Open cell 45nm Lib
Area (μm^2)	20423	47489	25182	93836	23910
Delay(ns)	3.51	4.00	3.70	2.59#	3.44
Area (μm^2) × Delay ^{2} $(ns)^2$	251613	759824	344741	629461	282941
Input-Output	Non-redundant	Non-redundant	Non-redundant	Redundant	Non-redundant

Redundant to non-redundant and vice-versa logic and its delay is not included in the design

Table 12 — Logical Hierarchical Placement in Nitro

Module	No of Cells	Cell Area in μm^2
FFT (TOP)	6839	10753
FFAS	1031	1170.13
Fmult x 2	2746	4111.55
Register files x 3	1623	3758.58
Mux 2:1 x 2	32	59.58
Mux 4:1 x 7	602	555.11
Controller	584	878.06
Program Memory	219	220.51

Table 13 — Design Summary of FFT Processor

Library	Nangate Open cell Library
Technology	45nm
Die Area	37251μm^2
Max Clock Frequency	500MHz
Standard Cell utilization	60.86 %
Power	4654.2μW
Total Cycles to compute 8-point FFT	76 cycles

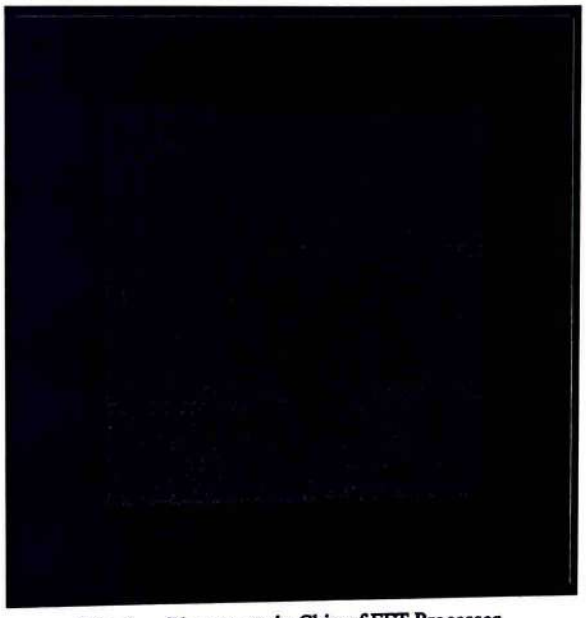

Fig. 5 — Placements in Chip of FFT Processor

Proposed processor dissipates 4.65 mW power. Operating voltage is 0.85V. The maximum clock frequency applied to this processor is 500MHz. The placement of logical cells is shown in Fig. 5. For fair comparison of proposed application specific integrated circuit (ASIC) design of FFT processor with previously reported designs having different FFT sizes, area-time complexity (AT^2_{norm}) , stated by Diego *et al.*[14] is used. Area-time complexity is the second order normalised term and given by Eq. 4, in which A, s, N and T represents area, processing technology in µm, FFT sequence size and time respectively.

Table 14 — Comparative Statistics of Hardware Utilization and Cost Metrics

Parameter	Proposed Design	Xiao *et al.*[6]	Velncia *et al.*[7]	Noor *et al.*[13]	Diego *et al.*[14]
Technology (T) nm	45	130	45	90	180
Area (A) μm^2	37251	2700000	348100	198404	740000
Voltage V	0.85	1.2	1.1	1.2	1.8
Clock Rate MHz	500	40	317	100	505
Power (D_p)mW	4.65	35.7	10	3.44	192
Data Length	16	10	16	16	8
FFT Points (N)	8	8192	32	128	12
AT^2_{norm} mm^2 ns^2	0.296	0.394	1.73	0.594	0.242
$AT^2_{norm} D_p$ mm^2 ns^2 mW	1.37	14.09	17.32	2.03	46.42

$$AT^2_{norm} = \frac{Area}{N\,(s/0.18)^2}\,T^2 \qquad \ldots(4)$$

The hardware cost metric is represented by the product of AT^2_{norm} and power (D_p).[14] The hardware cost metric of proposed processor is 1.37. Comparative statistics of hardware utilization and cost metric with previous work[6,7,13,14] is given in Table 14. The proposed processor dissipates more power as compared with the ASIC design reported by Noor *et al.*[13] It is worth mentioning that proposed processor has lowest hardware cost metric and AT^2_{norm} . The hardware cost metric is 32.51 % less as compared with hardware cost metric of ASIC design given by Noor *et al.*[13]

Conclusions

The proposed FFT processor can be suitably suitable to adopt in radix–r pipelined split radix architecture for small independent, radix-2, 8-point computation. Twiddle constants are implicitly available in instructions to avoid the additional fetch cycle for them. Intermediate computational result are stored in register files which saves the load and store time required in memory-based architecture. Computational unit i.e., BU of proposed FFT processor is formatting smaller. It replaces a set of two five operand adder and two multipliers by dual path fused floating point addition-subtraction, two floating point multiplier as compared with previous work. The proposed BU performs arithmetic computation in floating point form to reduce the

nonlinearities. Hence the proposed architecture reduces the MSE by 41.95% and 55.76% in magnitude and phase respectively as compared with computations performed by rounding the twiddle constants. The proposed processor also offers the flexibility to compute FFT in time and frequency domain without changing the BU design. It is also observed that hardware cost metric of the proposed architecture is 32.51% less than previous work.

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Indian pharmaceutical patent prosecution: The changing role of Section 3(d)

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Abstract

India, like many developing countries, only recently began to grant pharmaceutical product patents. Indian patent law includes a provision, Section 3(d), which tries to limit grant of "secondary" pharmaceutical patents, i.e. patents on new forms of existing molecules and drugs. Previous research suggests the provision was rarely used against secondary applications in the years immediately following its enactment, and where it was, was redundant to other aspects of the patent law, raising concerns that 3(d) was being under-utilized by the Indian Patent Office. This paper uses a novel data source, the patent office's first examination reports, to examine changes in the use of the provision. We find a sharp increase over time in the use of Section 3(d), including on the main claims of patent applications, though it continues to be used in conjunction with other types of objections to patentability. More surprisingly, see a sharp increase in the use of the provision against primary patent applications, contrary to its intent, raising concerns about potential over-utilization.

Keywords:- pharmaceutical, patents, Section 3(d), patent law.

Introduction

India began to allow pharmaceutical products to become patented in 2005, in compliance with the country's obligations under the World Trade Organization's Agreement on Trade-Related Aspects of Intellectual Property Rights (TRIPS). In doing so, the Indian government inserted a controversial provision into the patent law, Section 3(d), which tries to limit the grant of "secondary" pharmaceutical patents, i.e. patents on new forms of existing molecules and drugs.

Section 3(d) has been the source of considerable conflict. One prominent case that brought the world's attention to 3(d) was the Indian Patent Office's (IPO) decision to reject a secondary patent on Novartis' cancer drug "Gleevec" (imatinib mesylate), a decision that cited Section 3(d) as one of the grounds for rejection. Novartis challenged the constitutionality of Section 3(d) and appealed the IPO's decision, actions that in turn inspired health activists to embark on a campaign against Novartis and in support of the provision. The legality of 3(d) was upheld, and the decision to reject the Gleevec patent was confirmed by the Intellectual Property Appellate Board in 2009 and then, ultimately, the Indian Supreme Court in 2013.

Debates and controversies over 3(d) have not been limited to this one drug. The provision has triggered heated and polarized views on pharmaceutical patents in India, and more broadly in developing countries adopting pharmaceutical patents in compliance with TRIPS. On the one hand, many legal scholars, civil society groups, and international organizations have lauded India's policy choice, citing 3(d) as a prominent example of a country complying with its international obligations but doing so in a way that can preserve generic competition. In that spirit India's Section 3(d) is commonly held out as model to follow, and other countries where pharmaceutical patenting is also new are encouraged to act similarly. On the other hand, many foreign governments and the transnational pharmaceutical industry regard 3(d) with disdain. The US Government routinely cites 3(d) as among the reasons for including India on the "Priority Watch List" in the United States Trade Representative's annual Special 301 Report, for example, and the provision has drawn repeated criticism from international drug firms and their representatives. The concern that 3(d) makes it difficult to get a patent in India is widespread in the scholarly literature as well. However, these analyses did not look specifically at the role of 3(d) itself, but measures of patent protection on molecules which could be influenced by other factors, including the timing of TRIPS implementation in India.

Previous empirical analyses that did look directly at 3(d) found little independent role of 3(d) in shaping Indian pharmaceutical patent outcomes. Specifically, these analyses found that the provision was involved in a relatively small number of cases, and, where it was, it was almost always used together with other more conventional reasons for rejecting patent applications, such as lack of novelty or inventive step. However, the previous analyses were based on pharmaceutical application filings and examination decisions in the early years after the introduction of pharmaceutical patenting in India. It is possible that the role of 3(d) has changed over time, given implementation lags and updated guidance to IPO examiners. Moreover, where 3(d) and other grounds for rejecting patents were employed, previous analyses were unable to untangle which were the main reasons for rejection.

This paper uses new micro-level prosecution data to examine changes over time in 3(d) and to assess the independent role of this provision. While analyses of patent prosecution process are now common for applications filed at the United States Patent and Trademark Office., there are few empirical analyses of developing country patent prosecution. This is particularly crucial for analyzing patent prosecution in the context of TRIPS, given concerns that developing countries' practices may differ substantially from their laws on the books.

As we seek to understand how the patent office functions and, specifically, the role of Section 3(d) in patent prosecution processes, we focus not just on the IPO's final decisions, but also examiners' initial reports, as well as the exchanges that occur between applicants and the patent office following issuance of the initial reports.

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Focusing on the first examination reports (FERs) provides a fuller picture of the role of 3(d) in patent prosecution, allowing us to understand how 3(d) is used by examiners and how applicants respond to 3(d) objections that are raised in the course of examination. Another novel aspect of our approach is that we examine the role of 3(d) and other substantive grounds for rejection in targeting the first claim of patent applications. This allows us to assess whether 3(d) struck the core of the application, and whether it did so on its own or in conjunction with other aspects of patent law. Analyses of FERs, which we see relatively early in the prosecution process, also avoids the problem of censoring which complicates assessment of grant rates. This is particularly important for examining changes over time. There is a trade-off, however, as we do not see final decisions in most cases, as we discuss more below.

We find a sharp increase in the prevalence of 3(d) in FERs over time, including on applications' most important claims. However, 3(d) rarely works alone: it continues to be invoked along with other more conventional objections, even when it is used on an application's main claim. While the provision does appear to make obtaining a patent more difficult and the prosecution process longer, it is hard to know whether this is due to the independent effects of 3(d), the types of applications that draw 3(d) objections, or the types of examiners that invoke 3(d). Surprisingly, we also find evidence that 3(d) is more commonly used for primary patents than secondary patents, suggesting that it is functioning differently than intended.

The paper has 5 sections. Section 2 provides brief background and context on the introduction of pharmaceutical patents in India and Section 3(d), along with an overview of the patent prosecution process. Section 3 describes the data and empirical approach. Section 4 presents results, examining the changing utilization of 3(d) over time in FERs, the relationship between 3(d) and novelty and inventive step, the association between 3(d) in FERs and final outcomes, and the use of 3(d) on primary vs. secondary patent applications. Section 5 presents discussion of the main findings, indicates directions for future research, and links research on the role of Section 3(d) to broader issues regarding the implications of pharmaceutical patents in India for access to medicines in poor countries in the context of TRIPS.

TRIPS, pharmaceutical patents, and Section 3(d)

The World Trade Organization's (WTO) Agreement on Trade-Related Aspects of Intellectual Property Rights (TRIPS) requires all countries to grant pharmaceutical patents. With the exception of "Least Developed Countries," all WTO members that did not already allow pharmaceutical patents as of 1995, when TRIPS went into effect, had until 2005 to begin doing so. During the transition period, from 1995 until the date that a country made pharmaceuticals patentable, TRIPS required members to receive and hold applications in a "mailbox." Thus, if in a given country pharmaceutical patents were to become available as of 1999, from

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1995 to 1999 the country would accept applications in the mailbox, and these would be examined as of 1999, along with other applications received from that date onwards.

India was one of the countries that most resisted TRIPS during the Uruguay Round trade negotiations of the late 1980s and early 1990s. India opposed the inclusion of rules on countries' intellectual property policies and practices in the international trade regime, and once the "trade-IP" linkage was established and TRIPS negotiations began, India adamantly resisted the subsequent obligation that all countries allow pharmaceuticals to be patented. Although process patents were available in India, product patents had been prohibited since 1970. The absence of patent protection in India coincided with substantial development of the local pharmaceutical sector, and TRIPS was thus perceived as a serious threat. Perhaps not surprisingly, when forced to allow drug patents but allowed a transition period before doing so, India waited until 2005 to make pharmaceutical products patentable, the maximum period allowed. Indeed, India is one of the only countries to use the full transition period and delay pharmaceutical patenting until 2005. And, also in grudging compliance with the country's new international obligations, as of 1999 India also began receiving applications in a mailbox, to be examined as of 2005 when the product patent regime was in operation.

In 2005, at the point of introducing the final amendments to the Patents Act to allow for pharmaceutical patents, the Indian government included Section 3(d), a provision that establishes a high barrier for secondary patents. Specifically, 3(d) stipulates that many secondary patents are not considered as inventions, and thus not eligible for patents, unless the applicants demonstrate that these have greater efficacy:

The following are not inventions within the meaning of this Act... The mere discovery of a new form of a known substance which does not result in the enhancement of the known efficacy of that substance or the mere discovery of any new property or new use for a known substance or the mere use of a known process, machine or apparatus unless such known process results in a new product or employs at least one new reactant. For the purposes of this clause, esters, ethers, polymorphs, metabolites, pure form, particle size, isomers, mixtures of isomers, complexes, combinations, and other derivatives of known substance shall be considered to be the same substance, unless they differ significantly in properties with regard to efficacy.

Section 3(d) was implemented explicitly to address concerns that additional patents on existing substances could be used to extend market exclusivity and delay generic competition. Basheer and Reddy report that the Minister of Commerce at the time the patent law was being finalized introduced 3(d) to prevent "ever-greening". While some actors sought a more restrictive approach, for example prohibiting all secondary patents, the designers of 3(d) sought a middle ground that would allow patents on modified forms of existing compounds so long as they demonstrated improvements

("efficacy") over the earlier, known substance. This intermediate position was subsequently supported by a government-established committee that was asked to report on whether India should prohibit patents on all "incremental innovations".

Thus to obtain a pharmaceutical patent in India, not only do applicants have to satisfy traditional criteria that are common across all countries, e.g. novelty and inventive step, but also meet Section 3(d) requirements. As indicated in the introduction, Section 3(d) has received considerable attention, but its effects have tended to be exaggerated by both supporters and critics. We use micro-level data to shed new light on India's new pharmaceutical patent system and the role of 3(d).

Before proceeding to the data and analyses, a quick review of the Indian pharmaceutical patent prosecution process may be useful. Applicants must request examination by the IPO within 4 years after their application's international priority date; failure to do so leads to applications being classified as "withdrawn." When the IPO examines applications, a first examination report is typically issued within six months. FERs range from a few lines to long and detailed documents with extensive discussions of claims. FERs are like "first office actions" in the U.S., which list objections such as novelty and inventive step, as well as other less substantive grounds such as lack of clarity and mistakes in the application. If an applicant does not respond to the FER the application is "abandoned." When the applicant does respond, amending or eliminating claims, or rebutting the objections raised by examiners, the IPO then issues a second report and, typically, invites the applicant to a hearing. If the applicant overcomes these objections the patent is granted. If, however, the applicant stops pursuing the application after initially having replied to the FER, for example the applicant does not respond to the IPO's second report or does not attend the hearing, or does take these steps but is unable to convince the patent office of the merits of the case, the application is refused.

Data and empirical approach

We started with a set of pharmaceutical applications that were filed globally via the Patent Cooperation Treaty (PCT), both to focus on relatively important applications and to allow for comparability of Indian outcomes to those in other jurisdictions. Accordingly, we began with the September 2015 version of the OECD Triadic Patent Families database, which covers all applications filed in the European Patent Office, US Patent and Trademark Office, and Japanese Patent Office. Using this database, we focused on all "pharmaceutical" applications with priority years (first global filing years) 2000–2012. We then collected information from the WIPO statistics database on all Indian national stage applications; since at the time we collected the data the Indian data were truncated in 2012, we focus the subset with Indian applications filed through 2011. For tractability, we focus on applications with priority PCT month July. This resulted in 1,964 PCT applications, mapping to 1,993 Indian national stage applications. (Since India took full advantage of the transitional period to

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introduce pharmaceutical patents that was allowed by TRIPS, as explained above, the applications in our dataset that were filed in India from 2000–2005 were held in a "mailbox" until examination commenced in 2005.)

We collected Indian outcomes on all 2000–2011 applications from the Indian patent database as of May 2017. We record five mutually exclusive categories: applications can be granted, pending (still waiting final determination), withdrawn before examination, abandoned after a first examination report issued, or refused. As explained above, if an applicant pursues the application after receiving the FER but is unsuccessful in overcoming the objections raised, the application is considered formally refused. We also collect data on duration of prosecution for granted patents.

As explained, a novel contribution of our work is that we analyze the first examination reports issued by the patent office after applications have undergone their first substantive review. For all applications with FERs we determined if the reports included any 3(d) objections, and also whether they included any novelty or inventive step objections. We also determined whether there were 3(d) objections on the first claim, and, for a subset of applications, whether there were novelty or inventive step objections on Claim 1 as well.

While most of our analyses of 3(d) focus on FERs, we also use the full prosecution record of some applications to gain a stronger sense of the role of 3(d). For all applications where there was a 3(d) objection on claim 1 of the FER and a final outcome of refusal, and for a random selection of applications with 3(d) objections on claim 1 that ultimately were granted by the patent office, we read through the correspondence between applicants and the patent office (e.g. replies to FERs, subsequent examination reports, controller's reports) to understand how applicants respond to 3(d) objections and the role of 3(d) throughout the prosecution process.

To examine the different roles of 3(d) for different types of applications, we code each of the applications in our sample as to whether they claim a new compound ("primary" patent applications) or, alternatively, a modified form, composition, or use of an existing compound ("secondary" patent applications) using the coding scheme from previous research. The claims coding also revealed a handful of pure process applications. After dropping these we were left with 1853 applications.

Results

We use these data to address the following questions:

- How has the use of 3(d) by examiners in FERs changed over time?
- How much overlap is there between 3(d) and novelty/inventive step objections in FERs?
- How does the inclusion of 3(d) objections in FERs, alone or in conjunction with novelty or inventive step, correlate with different outcomes?

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- What kinds of patent applications draw 3(d) objections in FERs?
- The changing role of 3(d) over time

To examine the role of 3(d) over time, we focused on applications that have FERs. The share of applications with an FER drops over time (for example, from about 78 percent in the 2001–2004 period to 52 percent in the 2008–2011 period). This is not surprising, as examination has not yet begun on a larger share of more recent applications. We were able to locate FERs for nearly all abandoned, granted, and refused applications (as well as a third of the pending applications, where examination has begun but not yet concluded), yielding 1,283 FERs. Overall, 37 percent of the applications with FERs are granted, 45 percent abandoned, 5 percent refused, and 13 percent pending.

The solid line in Fig 1 shows the share of applications with an FER with any 3(d) objection, by application year. The sharp increase over time, from less than 40 percent of the early applications to more than 80 percent of the most recent applications, demonstrates an increased utilization of 3(d) by Indian patent examiners. While previous research, based on even earlier sets of applications, revealed a low incidence of 3(d), this is clearly no longer the case.

Is 3(d) redundant?

The data presented so far suggest that 3(d) is a major way in which the Indian Patent Office tries to limit patent grants, and increasingly used over time. This is consistent with concerns that 3(d) makes it harder to obtain patents in India than other jurisdictions (as it was meant to do). However, one wrinkle is that we do not know what work is being done by 3(d) itself. Examiners may also be objecting to patents on other, more traditional grounds, such as lack of novelty or inventive step. Indeed, previous research has suggested just that, that Section 3(d) was rarely used alone, but rather in conjunction with other ways of rejecting applications. We explore this here too, both overall and for the main claim. Specifically, we also identified novelty and inventive step objections on the 427 FERs for applications filed between 2006 and 2007. We focused on applications for which there were electronic FERs, dropping 9, leaving 427. An advantage of looking at this time period is that the applications are more likely to have FERs (86 percent do) and the FERs are more likely to have clearer delineation of specific objections on specific claims.

What kinds of applications get 3(d) objections?

Previous analyses of 3(d) have focused mainly on its effects on secondary patent applications, which is natural since these are the applications it was meant to target. Together with the results (above) on the growth of 3(d) objections, prominent cases of 3(d) being used against primary patents (including, in a preliminary ruling, sobusfovir)—those covering drugs' original molecules–raise the question of whether it is being used more expansively.

Here we return to the full sample of applications with FERs (not just 2006–07), and we use our coding of whether the applications are primary or secondary. As

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noted above, and discussed in more detail elsewhere we categorize as "primary" applications those that include at least one claim on a new compound. Secondary applications include those on polymorphs and crystal forms, enantiomers and isomers, salts, metabolites and derivatives, and other modified forms, compositions, or uses of an existing compound that do not also have a new compound claim.

Discussion and conclusion

The data reveal substantial increases in the use of 3(d) over time in FERs, overall and with specific regard to the main claim. Clearly, the IPO is relying extensively on 3(d) to raise a higher barrier for obtaining pharmaceutical patents.

While the increased reliance on 3(d) may reflect characteristics of the applications filed in India, this may also reflect explicit policy. In the initial years of India's new pharmaceutical patent regime, many observers asserted that, notwithstanding the high-profile Gleevec case, 3(d) tended to be under-utilized. The association representing India's leading pharmaceutical firms published a report, authored by the former director of intellectual property in the Ministry of Commerce calling for more aggressive application of Section 3(d), for example, and subsequently worked with the IPO to revise the examination guidelines to that effect. And the defense of 3(d) provided by the Appellate Board and then the Supreme Court may have contributed to this too, by giving examiners greater confidence to use this provision. It is difficult to ascertain the effects of constituent pressures, revised guidelines, and legal support, though it is reasonable to believe they have contributed to the increased use of 3(d).

But Section 3(d) is rarely used alone. Even when 3(d) is invoked as a reason why a patent should not be granted, it is rarely invoked as the only reason. Examiners also use other, traditional, grounds to deny patents, such as lack of novelty or inventive step. Previous work, at the application level, suggested that this was common, and the current findings, based on FERs, are consistent with that research: looking at applications filed in 2006–07 for which we could obtain FERs, we find that when 3(d) objections are raised, in nearly all (94 percent) instances so too are objections based on lack of novelty or inventive step.

Overlap between 3(d) and other patentability criteria at the application level does not necessarily imply redundancy in use, as different provisions of the patent law may be applied to different claims within a single application. Researching the use of 3(d) and other provisions at the claims level is difficult, on account of the quality of FERs. In the initial years of patent examination FERs tended to be too vague, simply indicating that "claims" do not satisfy the tests of 3(d) or other aspects of the patent law, without indicating which claims a given objection was referring to. Looking at a set of applications during the time period when FERs tended to be more specific (but early enough so that FERs have been produced), our findings at the claims level are consistent with what we observed at the application level: in nearly all cases of 3(d) being used against the first claim in an application, so too were

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